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QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	09/105,739	Prepared by	NPB	Tracking Number	05891139
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JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE

Please provide new clean copy of claim pages dated 11/4/03 - page 8 and page 10. (data missing - see attached).

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RESPONSE

New pages 8 & 10 provided.

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E-5 (Rev. 10/01/02)

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TELECOPY MESSAGE

FOR: Examiner Janet Higgins

COMPANY: USPTO

FROM: Daria Gibbons for Jack Friedman

DATE: 3/26/04

NUMBER OF PAGES TO FOLLOW: 3

MESSAGE: I put in page 9 for good measure — portion of Supplementary Amendment originally faxed 11/4/03, S/N 09/105,739

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TELECOPY DESTINATION PHONE NUMBER:

18. (Original) The method of claim 17 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer.

19. (Original) The method of claim 17 wherein the first layer comprises a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer.

20. (Original) The method of claim 17 wherein the step of depositing capacitor fill material comprises performing a first deposition of capacitor fill material, recessing said first deposition of capacitor fill material, said recess partially exposing sidewalk of said capacitor trench, forming sidewall spacers on said exposed sidewalk of said capacitor trench, and refilling the capacitor trench and oversized capacitor opening.

21. (Original) The method of claim 17 wherein the capacitor fill material comprises n+ doped polysilicon.

22. (Original) The method of claim 17 wherein the step of diffusing dopants from said capacitor fill material into said semiconductor substrate from said lip of capacitor fill material comprises annealing the semiconductor substrate.

23. (Original) The method of claim 17 further comprising the step of etching an isolation trench, wherein said etching of said isolation trench removes a portion on said lip of capacitor fill material except where a connection between said capacitor and said transfer device is to be made.

24. (Original) The method of claim 23 further comprising the step of filling said isolation trench with isolation material and planarizing said isolation material.

25. (Original) The method of claim 24 wherein the first layer comprises a gate dielectric layer, a

gate conductor layer and a insulator layer and wherein the step of planarizing said isolation material removes said insulator layer to expose said gate conductor material.

26. (Original) The method of claim 24 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer and wherein the step of planarizing said isolation material leaves a portion of the insulator layer covering the gate conductor layer.

27. (Original) The method of claim 25 further comprising the step of depositing a wordline material layer on said gate conductor material and said isolation material, and further comprising the step of patterning the gate conductor material and wordline material to form a plurality of transfer device gates.

28. (Original) The method of claim 26 further comprising the steps of etching an opening in the remaining portion of the insulator layer to expose a portion of the gate conductor layer and depositing a wordline material layer on the exposed gate conductor material, the remaining insulator layer and the isolation material, and further comprising the step of patterning the gate conductor material and wordline material to form a plurality of transfer device gates, wherein the remaining insulator layer serves as an etch block to prevent unwanted etching of the gate conductor material.

29. (Original) The method of claim 24 wherein the first layer comprises a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer wherein the step of planarizing said isolation material removes any remaining portion of said second silicon dioxide layer and planarizes said silicon nitride layer, and further comprising the step of removing said silicon nitride layer and forming a gate dielectric layer, a gate conductor layer, and a wordline material layer, and further comprising the step of pattering said gate dielectric layer, said gate conductor

layer and said wordline material layer to define a gate of the transfer device.